ABSTRACT

Peripheral Component Interconnect (PCI) device contains Host Messaging Unit (HMU) which is operative to off load host processor and PCI device processor from PCI bus transfer overhead. HMU is configurable to asynchronously retrieve host processor commands from circular buffer, either by using polling or interrupt service techniques. Both host command retrieval methods are operable to remove host processor and PCI device processor from direct PCI bus command transactions, thereby increasing the efficiency of both processors. Interrupt service control of HMU is operative to buffer multiple service requests from PCI device processor, so that a more efficient use of the host processor interrupt service routine is implemented, providing for multiple service requests to be serviced in a single interrupt service request.